Analyze and Optimize 32- to 56- Gbps Serial Link Channels

January 26, 2017

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KEYSIGHT TECHNOLOGIES

wildriver technology

XILINX ALL PROGRAMMABLE.

AGENDA

Jack Carrel

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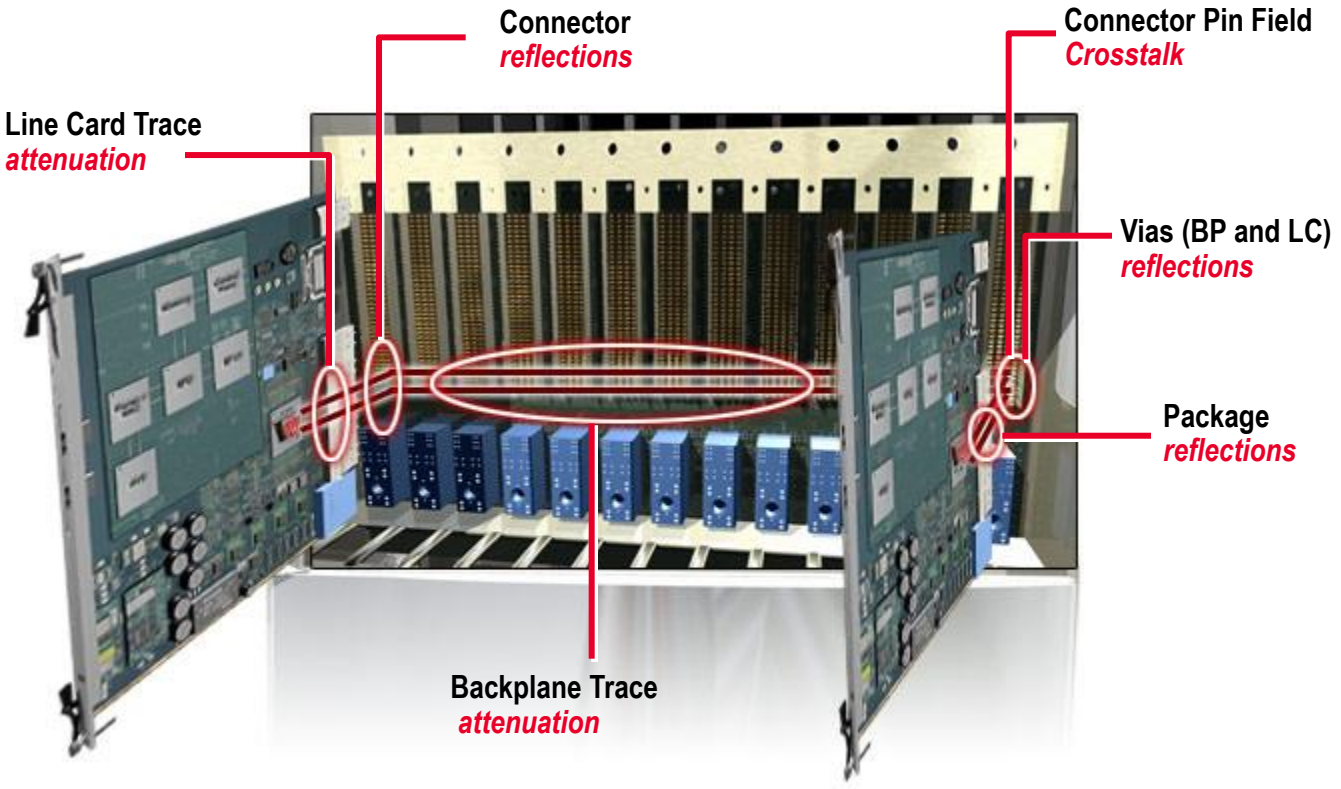
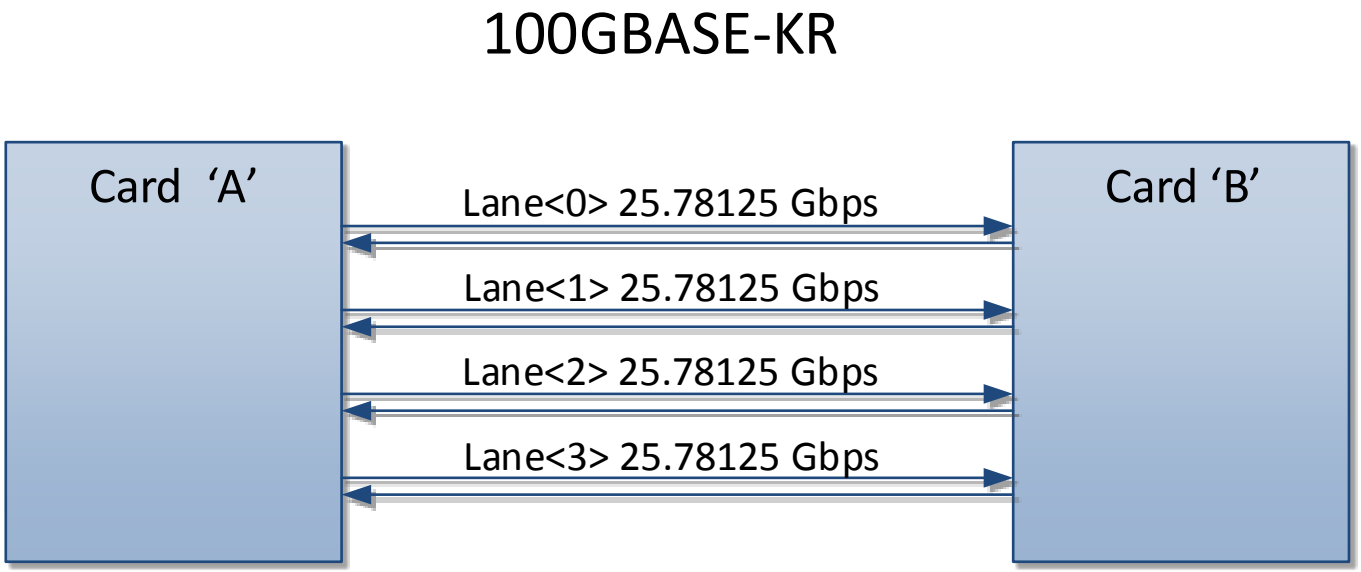
- Test Strategies for SerDes Channels
- Forensic Channel Analysis
- Gaining Insight with the Pulse Response

Serial I/O Channel – Backplane Channel



100GBASE-KR Backplane Interface



100GBASE-KR Backplane Channel

IEEE Std 802.3-2015
IEEE Standard for Ethernet
SECTION SIX – Annex 93B

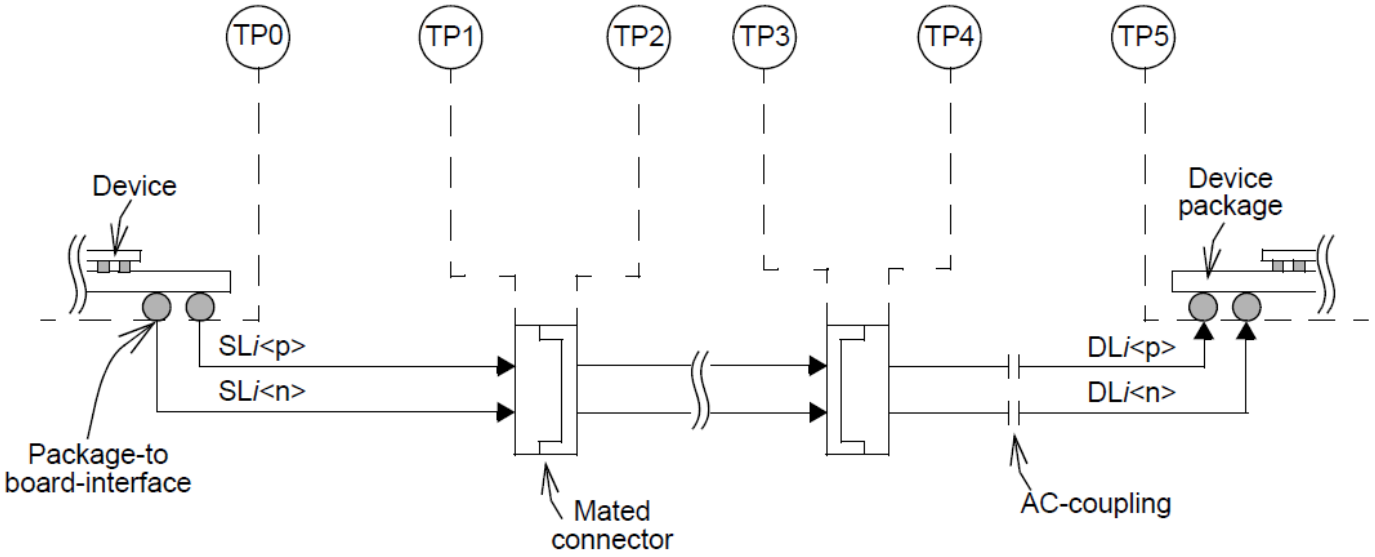


Figure 93B–1—Reference model (one direction from one lane is illustrated)

100GBASE-KR: Channel Testing

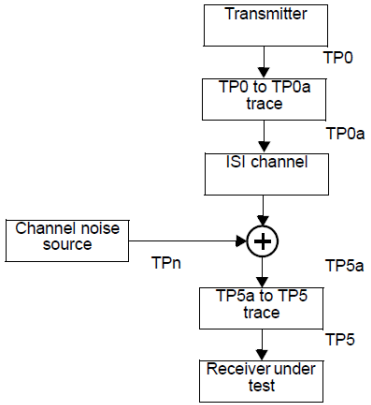


Figure 93C–2—Interference tolerance test setup

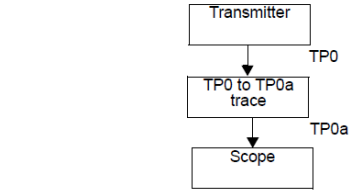
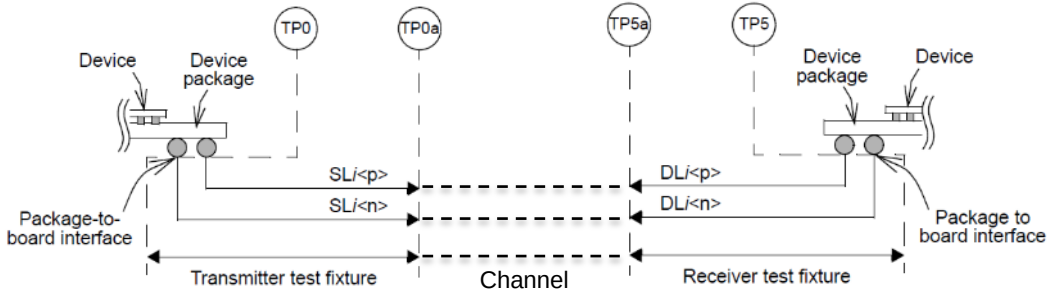
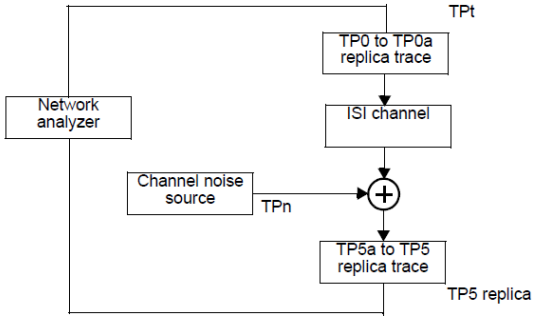


Figure 93C–3—Interference tolerance transmitter test setup





IEEE Std 802.3-2015
IEEE Standard for Ethernet
SECTION SIX

Figure 93C–4—Interference tolerance channel s-parameter test setup

100GBASE-KR: Channel Spec's

IEEE Std 802.3-2015
IEEE Standard for Ethernet
SECTION SIX

$$IL(f) \le \begin{cases} 1.5 + 4.6\sqrt{f} + 1.318f & 0.05 \le f \le f_b/2 \\ -12.71 + 3.7f & f_b/2 < f \le f_b \end{cases} \quad \text{(dB)}$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$IL(f)$ is the insertion loss at frequency f

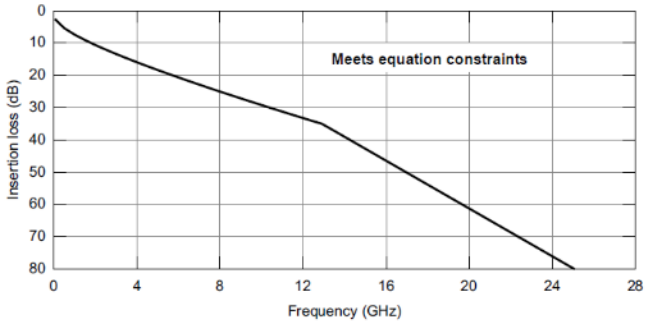


Figure 93–13—Insertion loss limit

$$RL_d(f) \ge \begin{cases} 12 & 0.05 \le f \le f_b/4 \\ 12 - 15\log_{10}(4f/f_b) & f_b/4 < f \le f_b \end{cases} \quad \text{dB}$$

where

f is the frequency in GHz
f_b is the signaling rate (25.78125) in GHz
$RL(f)$ is the return loss at frequency f

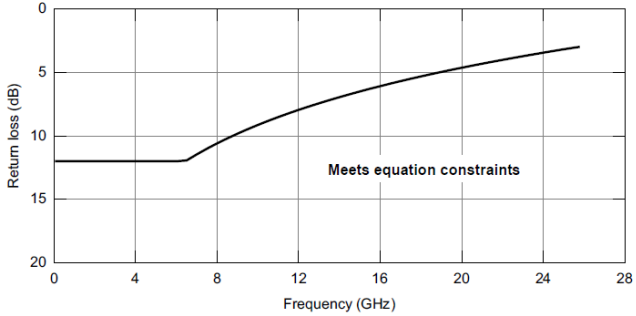
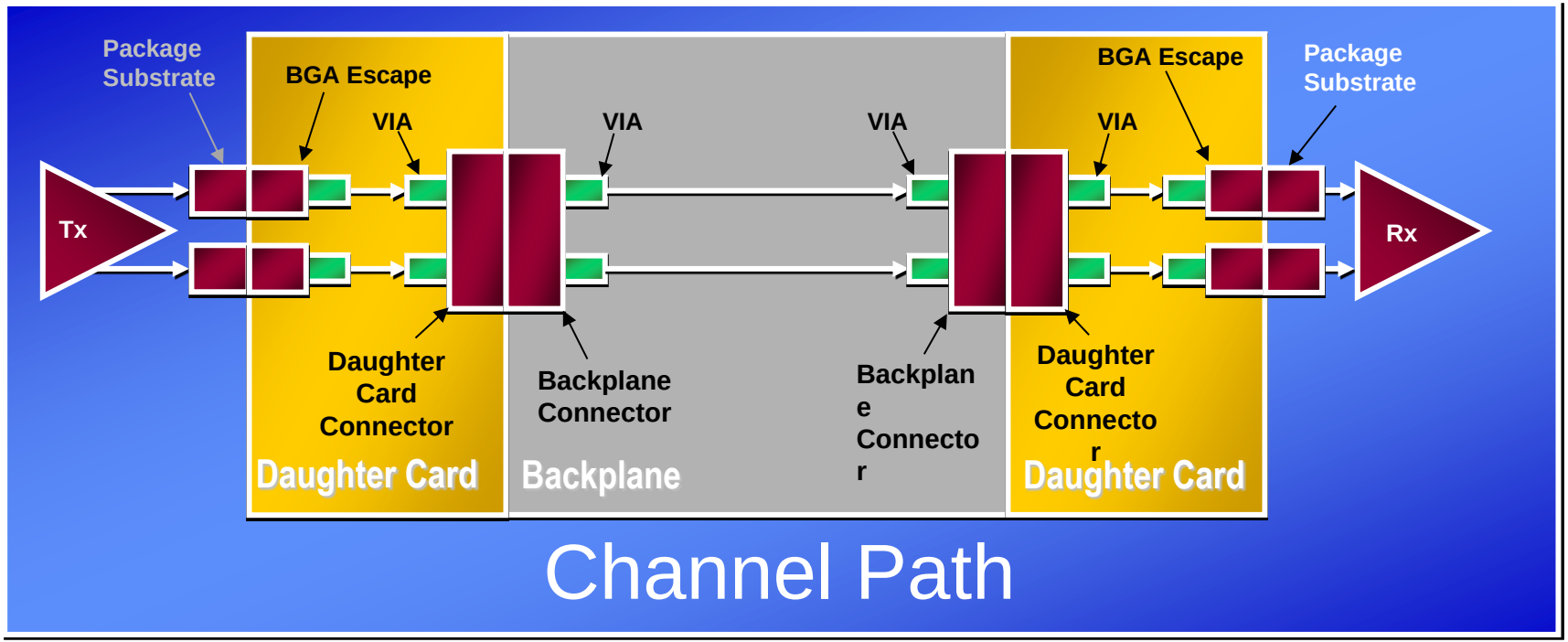


Figure 93–14—Differential return loss limit

100GBASE-KR: Channel Path Details – 1 Lane



100GBASE-KR: What's next?

- "No battle plan survives contact with the enemy"
  - Helmuth von Moltke

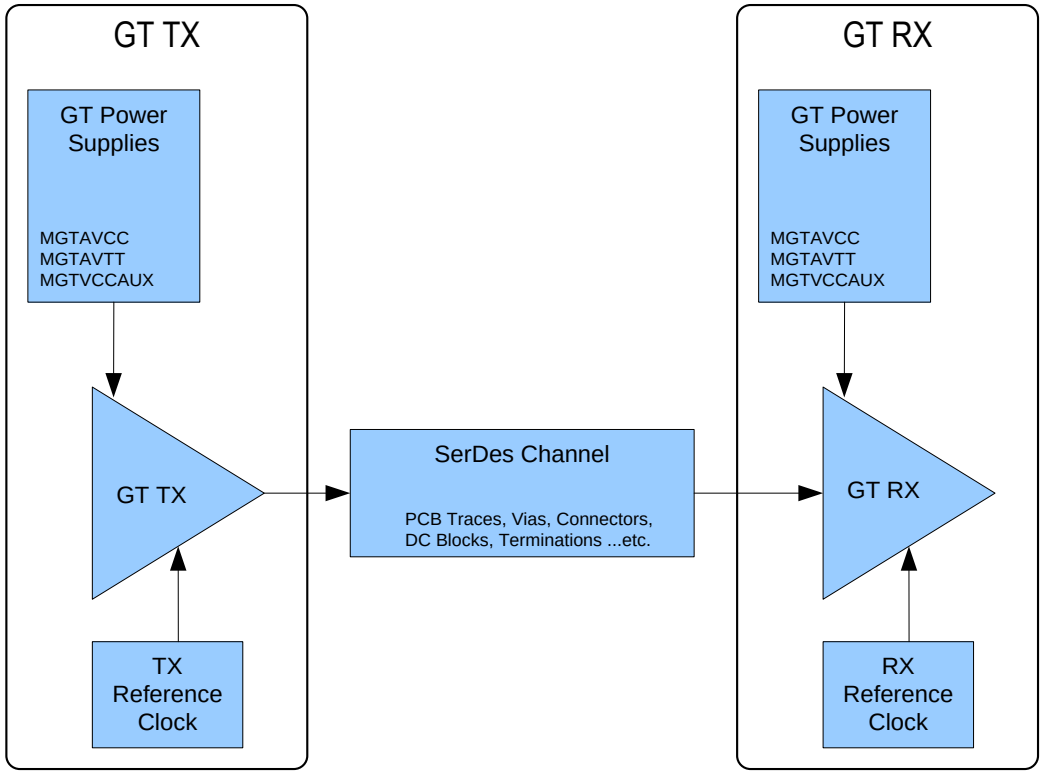
- "Everyone has a plan 'til they get punched in the mouth"
  - Mike Tyson

What if the link doesn't work?
"Stay Tuned"

SerDes Link Debug – bits & pieces

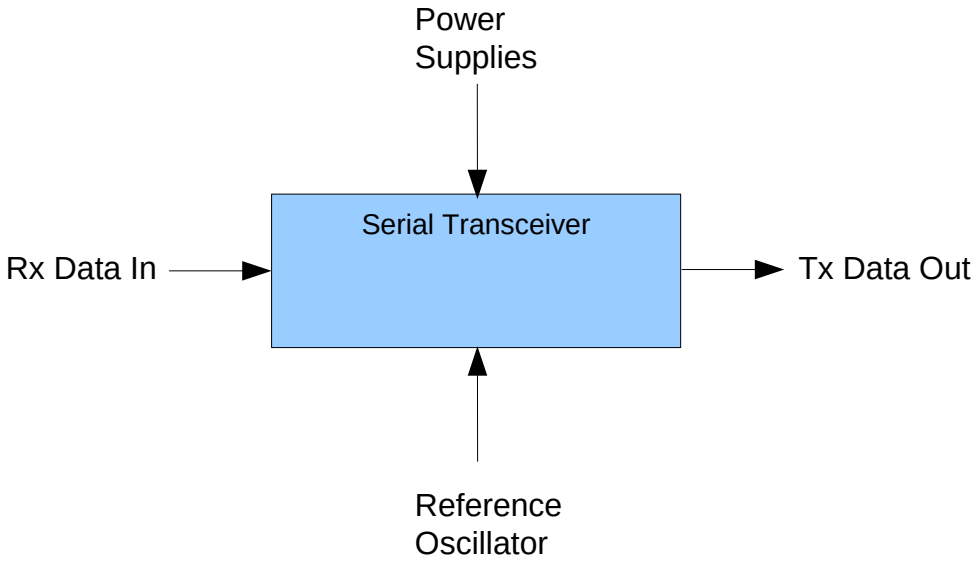
- Power Supplies
  - MGTAVCC
  - MGTAVTT
  - MGTVCCAUX
- Transmitter
- Receiver
- Reference Clock

- ***Verify connectivity***
- ***Verify compliance***



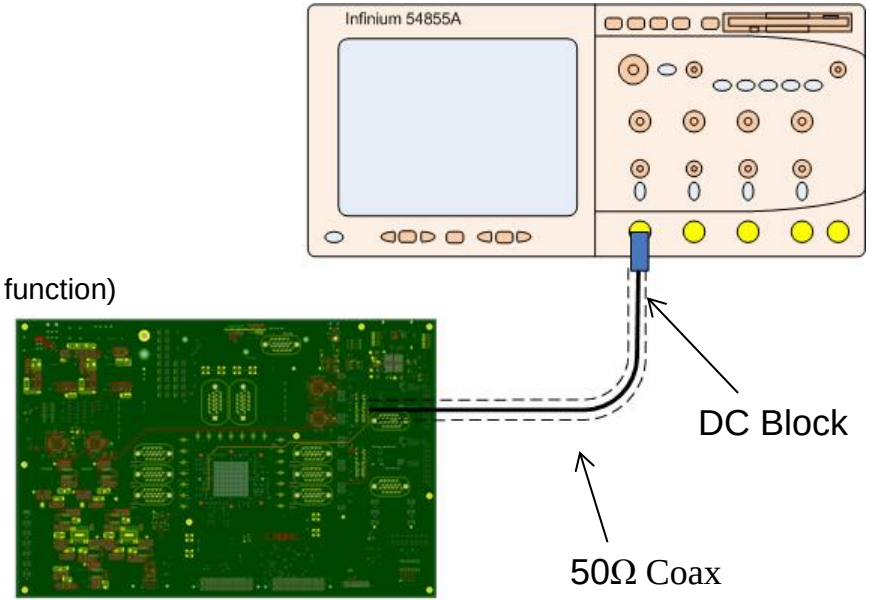
SerDes Link Debug – 4 Port Device

- Power Supplies
  - MGTAVCC
  - MGTAVTT
  - MGTVCCAUX
- Transmitter
- Receiver
- Reference Clock



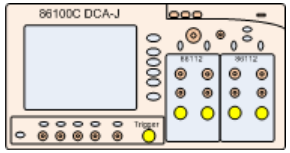
SerDes Link Debug – Power Supply Measurements

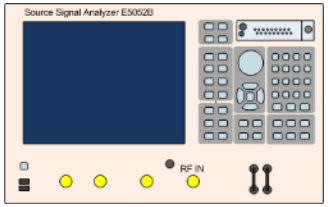
- Use 50 ohm probing. Using 50 ohms makes it easy to have a constant impedance for the entire path from the DUT to the oscilloscope input.
- Band limit the measurement. Limiting the bandwidth will
  - Reduce confusion from out-of-band energy.
  - Allows for easier detection and interpretation of measured waveform. (i.e. observe only what matters)
- To band limit, use a low-pass filter by using either
  - External low-pass filter between the DUT and scope input
  - Math processing function on the oscilloscope (Low-pass filter function)



SerDes Link Debug – Clock Measurements

- Clock measurements
  - Use TX output to measure clock frequency and phase quality
  - Use alternating pattern of equal numbers of one's and zero's to generate 'square wave'.
    - Frequency dependent channel losses are mitigated with alternating high-low pattern.
    - Pattern dependent distortion is minimized
  - Time Domain
    - Use scope with Jitter analysis package to measure Rj from TX square wave pattern.
    - Besides Rj look for Pj. Existence of Pj may be caused by interference (i.e. power supply noise, crosstalk, etc.)
  - Frequency Domain
    - Use Signal Analyzer or Spectrum Analyzer with phase noise package
    - Measure phase noise
      - Observe noise up to PLL tracking frequency (~1 to 10MHz)
      - Look for significant spurs at higher frequencies.
      - Calculate Rj for sanity check (Most instruments will do this for you.)





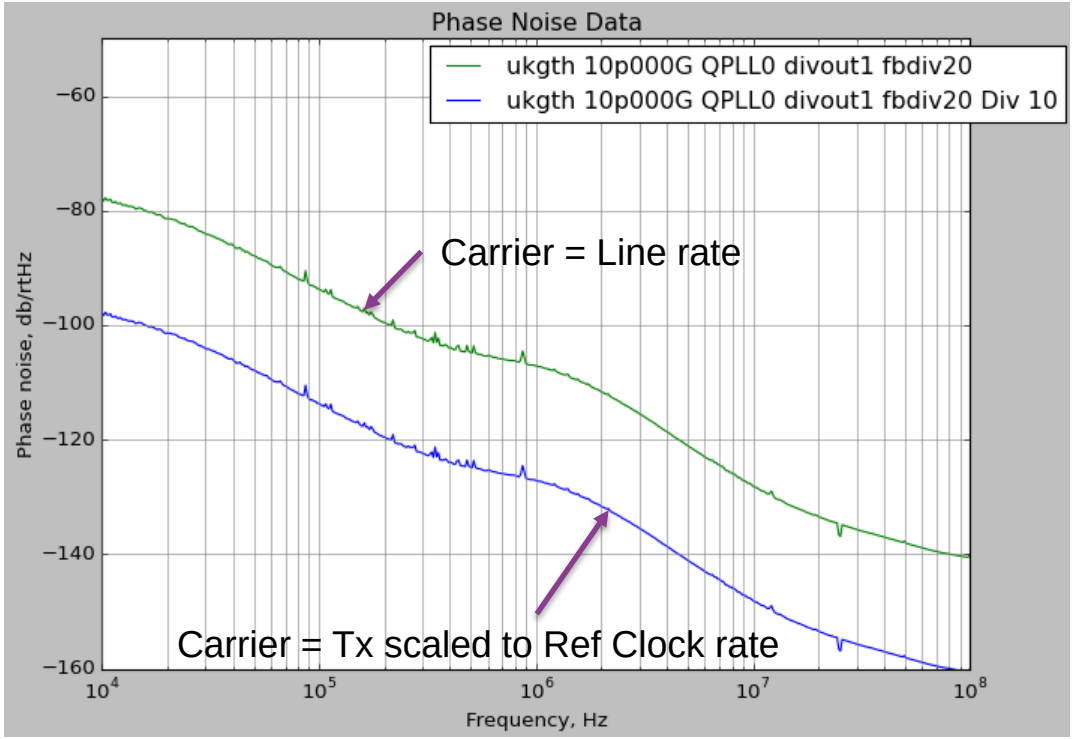
SerDes Link Debug – RefClk Phase Noise

UltraScale GTH

RefClk: 500.0 MHz
Line rate: 10.0 Gb/s

Scale phase noise to carrier Frequency:

$$\text{dB} + \left[20 \bullet \log_{10}\left[\frac{F_{OUT}}{F_{IN}}\right]\right]$$



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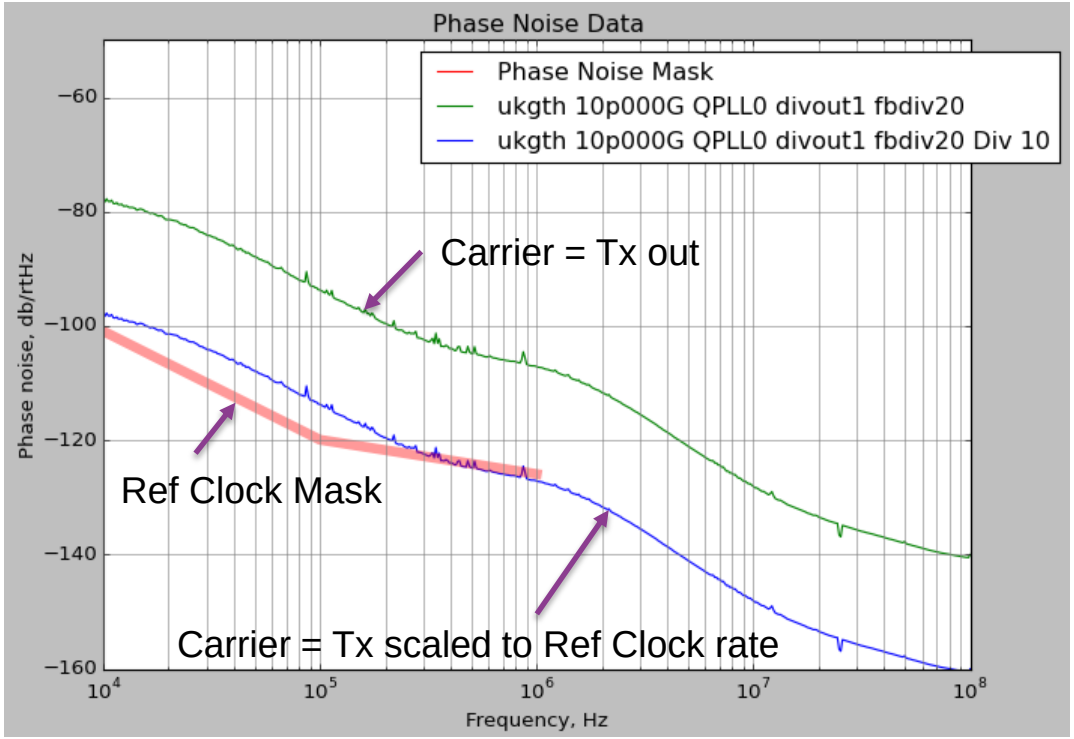

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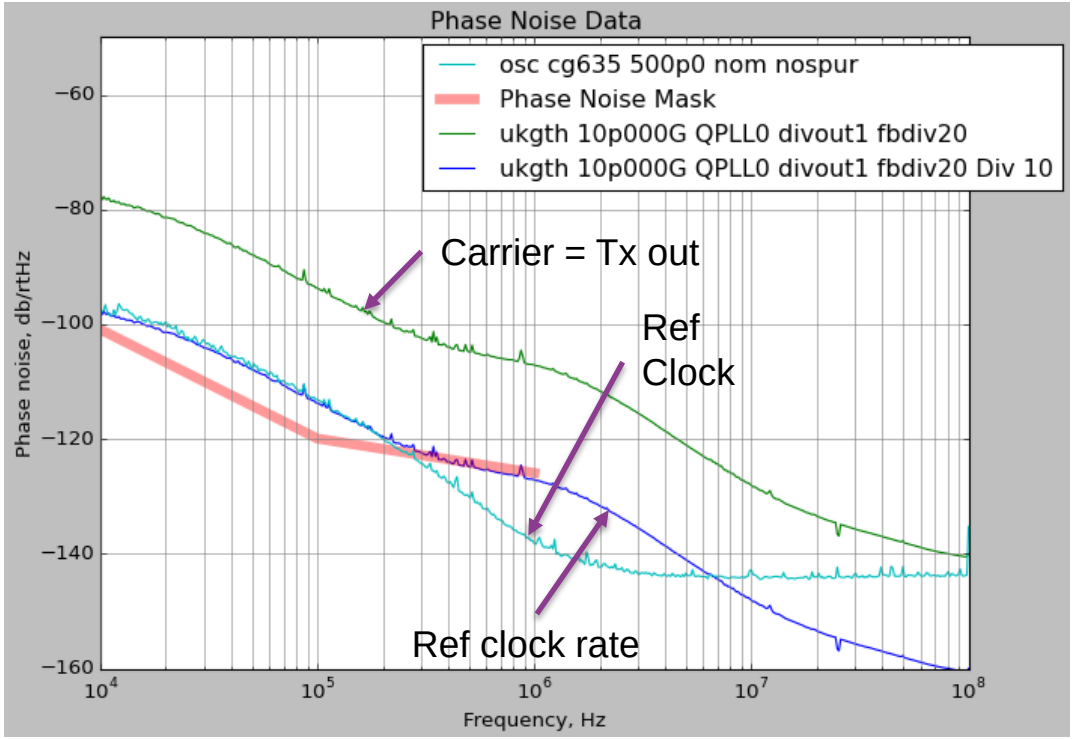

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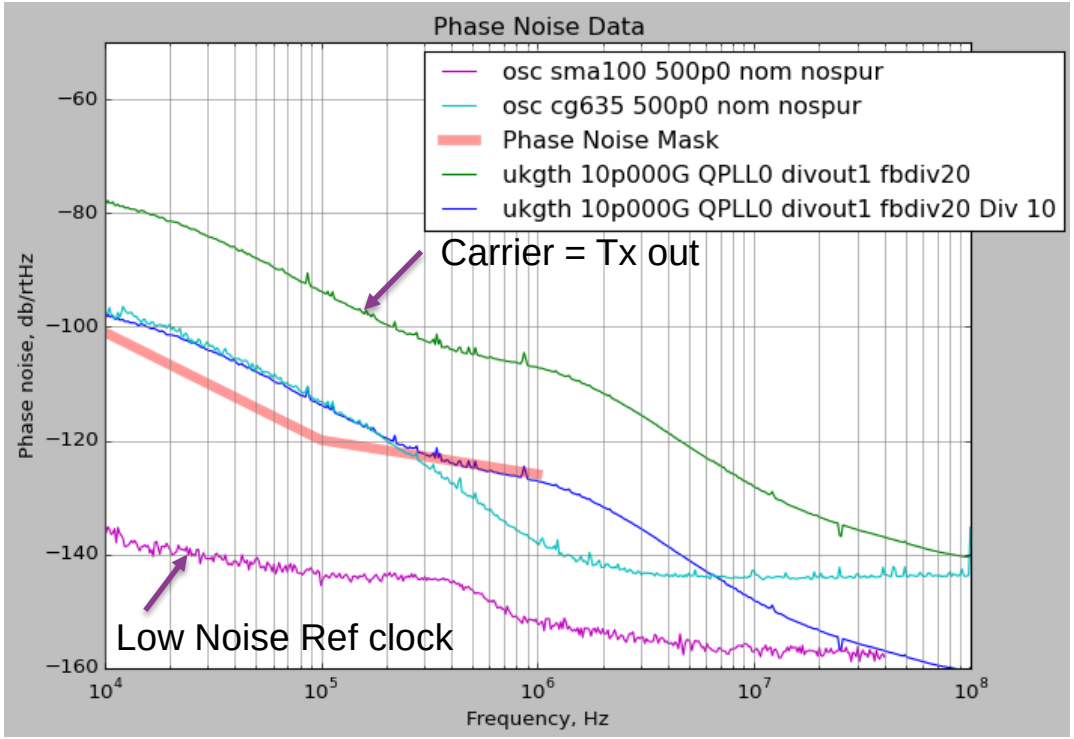

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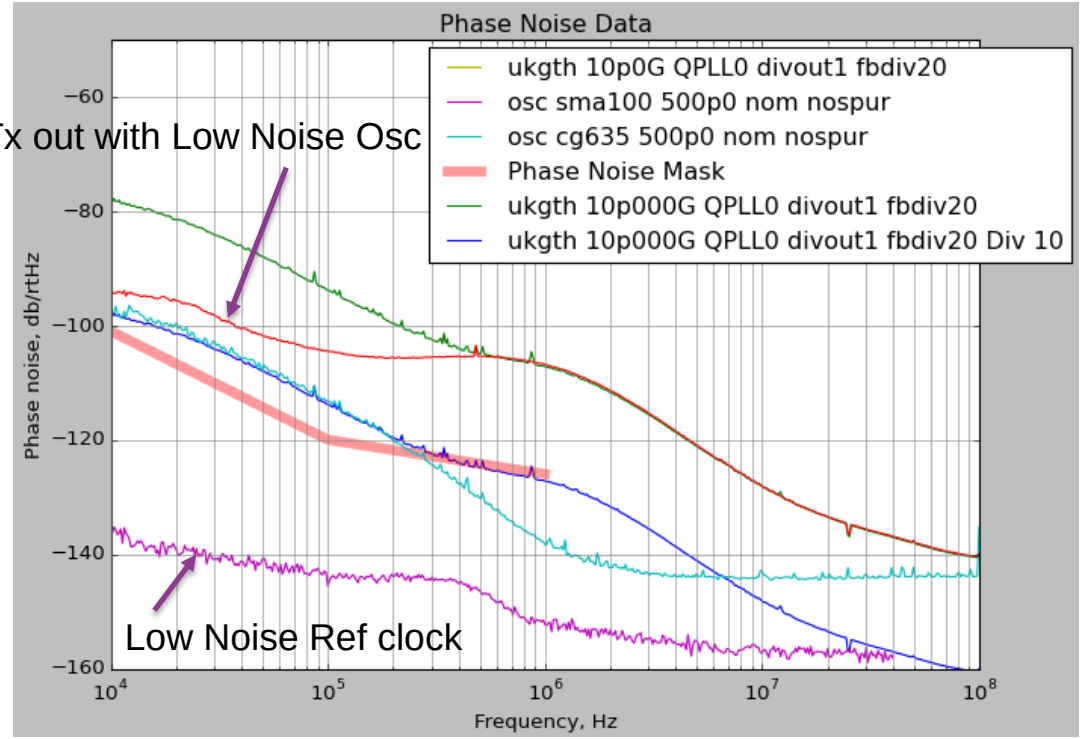

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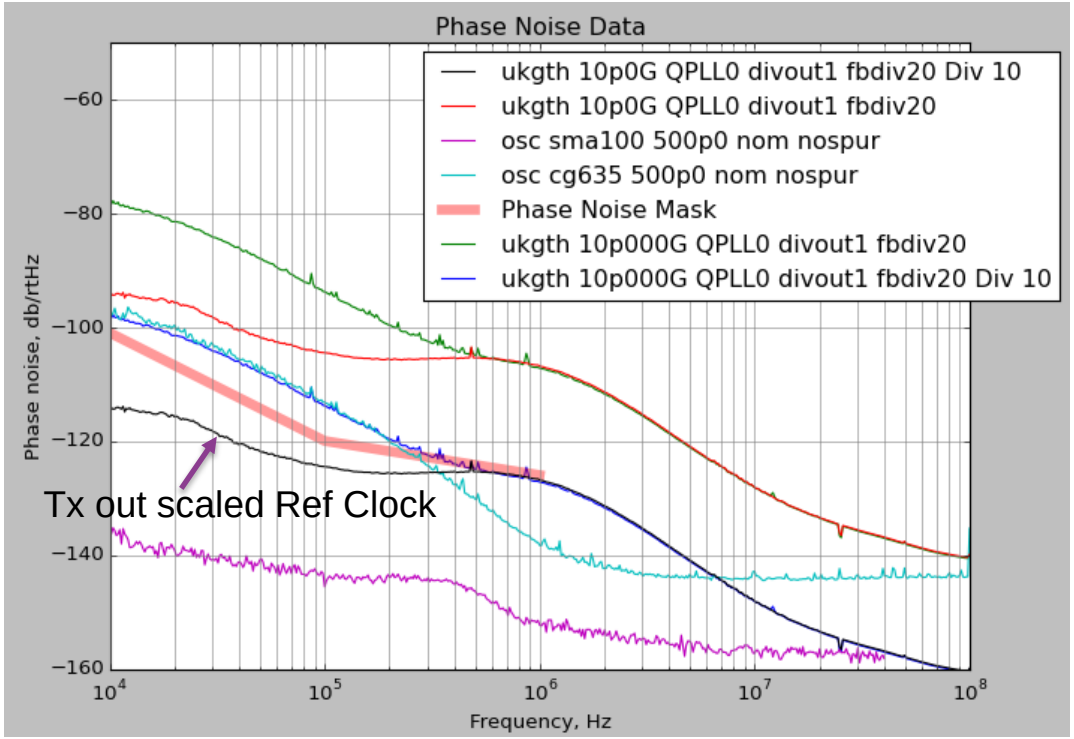
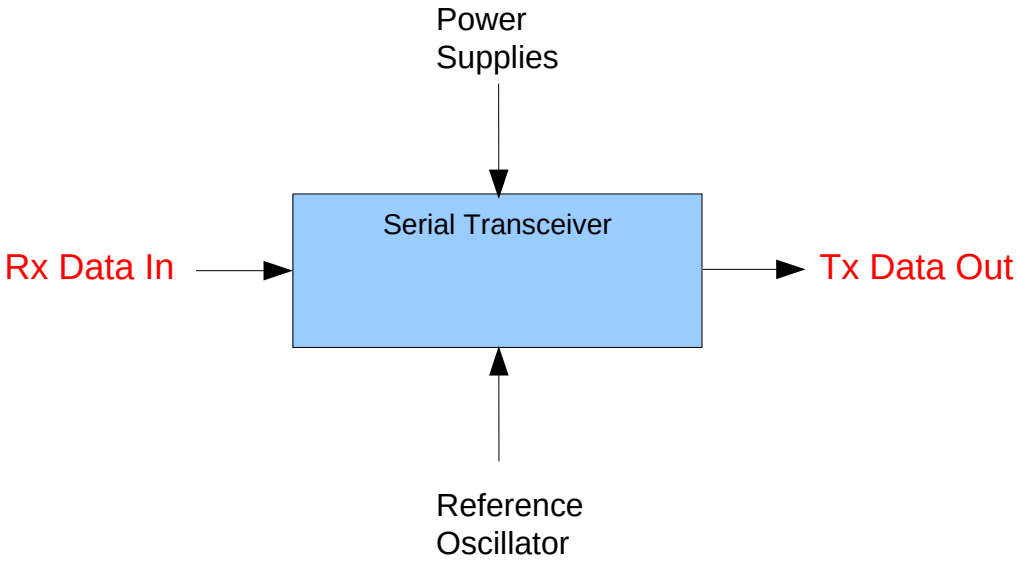


SerDes Debug – The Channel



…And now let's talk about
The Channel

AGENDA

Al Neves

Chief Technologist
Wild River Technology

- Test Strategies for SerDes Channels
- Forensic Channel Analysis
- Gaining Insight with the Pulse Response

Pathological Design Space – Advancing optimization and characterization

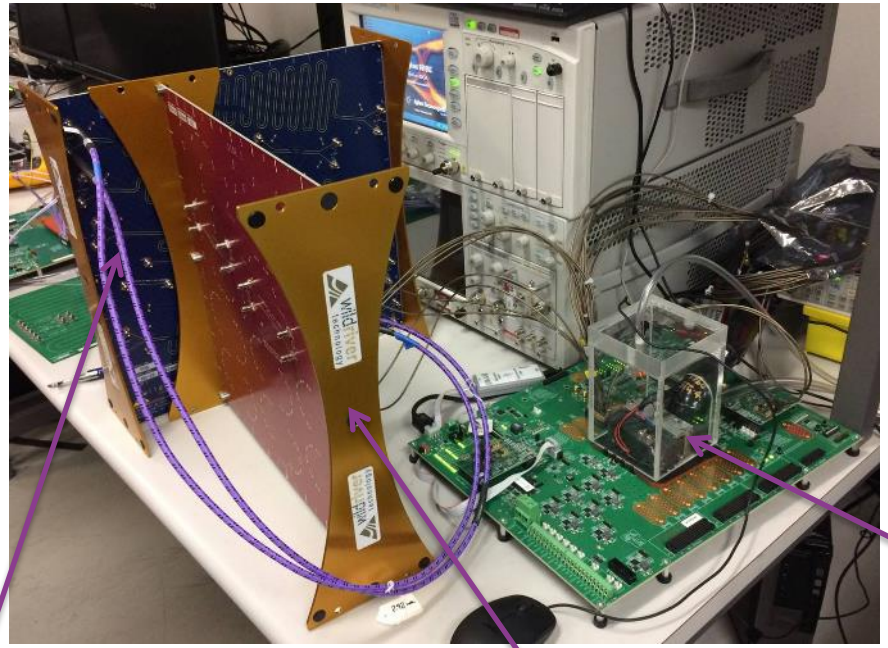
- Backplane characterization is a requirement
- Backplanes are, however, very complicated
- Difficult to form a coherent optimization strategy
- Difficult to establish clear margins versus issues

- *Good Engineering starts simple and systematic!*

“It’s all about the margins…”

Jack Carrel

Pathological Design Space – Guiding Principles



- Replace backplane with simple pathological structures.
- Structures can be systematically added
- Re-optimization for new and simple channel, then…
- Analysis of margin

XTALK-32 Crosstalk Platform

ISI-32 Loss Platform

UltraScale+ TX and RX, 32Gbpsec NRZ

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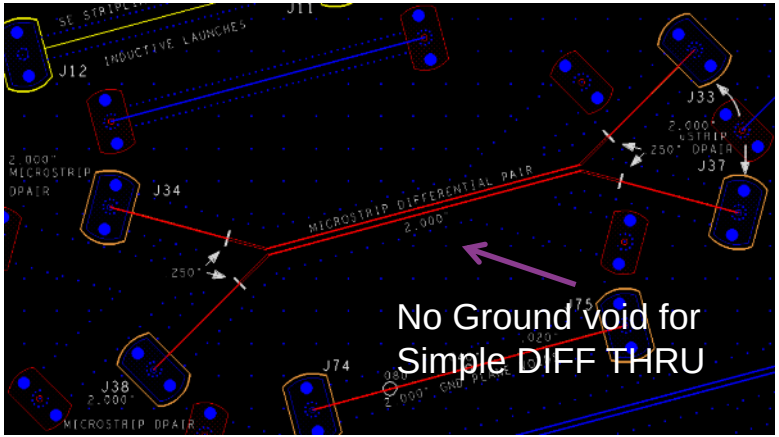
Pathological is an Analogous Concept

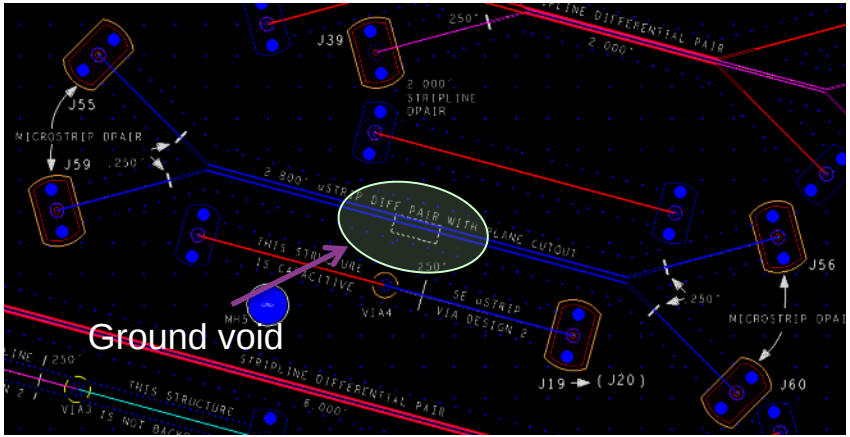
- For our application it denotes a stellar signal integrity structure with something with intentional poor S.I. added
- The overall structure itself, aside from the pathological element, is healthy with good signal integrity

Pathological Channel Concept – What is it?

- It is a family of interrelated structures
- There is always a root structure (like a THRU)
- Except for a single pathology, the structure is high S.I. (launches, transitions, fiber weave… etc.)

Pathological Channel Concept – Example





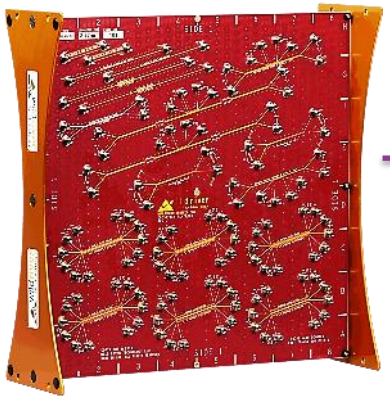
- **2inch DIFF microstrip THRU**
- Good signal integrity and low loss
- *Also used for 2X THRU for AFR and Measure Based Modeled de-embedding structure on right*

- **2inch DIFF microstrip THRU Exact Copy of left + Asymmetric Ground Void**
- Results in SDD11 degradation and mode issue of SCD21

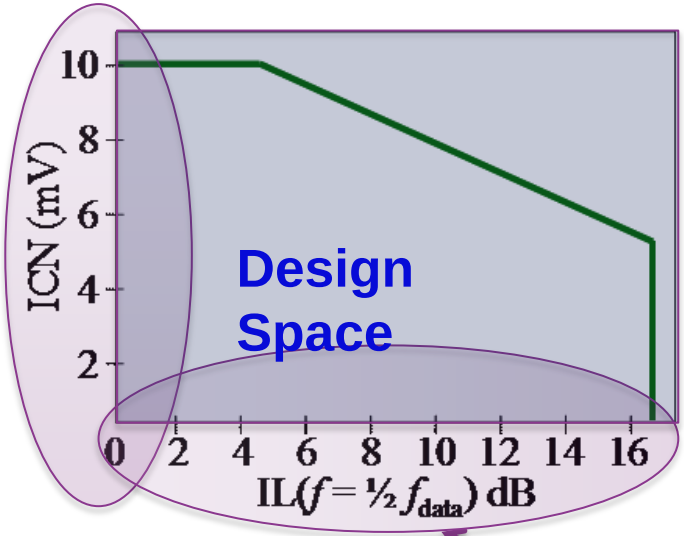
Pathological Design Space - Benefits

- Improve SERDES characterization
- Ability to Improve manufacturing (Test, Product, and Characterization Engineering) and design process
- Drive technology tweaks and next generation products
- Provides systematic approach over complete design space of all pathologies
- Improve Measurement-Simulation correspondence
- Test IBIS AMI models over full Pathological space

Pathological Design Space Concept – 2-D Space



Crosstalk Noise Test vehicle, calculated RX noise as Integrated Crosstalk Noise (ICN)



Loss and Crosstalk combinations can be mapped over the entire design space

Insertion Loss Test Vehicle (IL) at Nyquist Sampling Freq

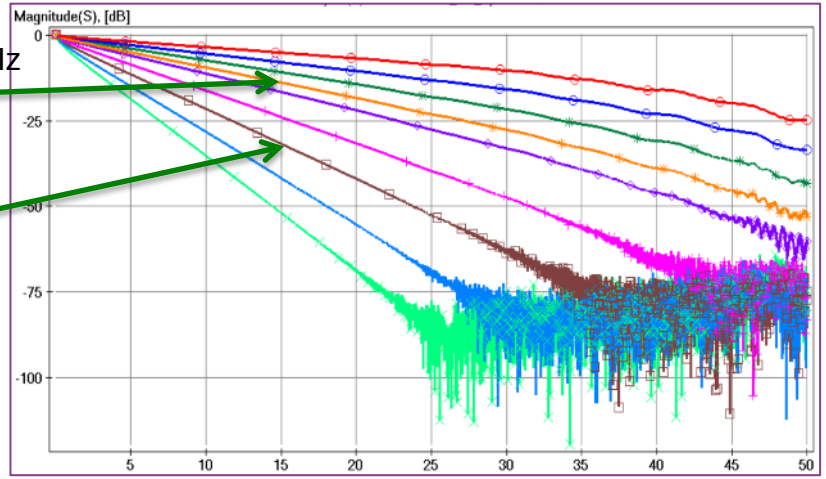
Pathological Space – Loss Example

START: Clean Pristine Low-Loss Channel

-13dB @15GHz

-30dB @15GHz

+Moderate Loss



- **+ RJ** → next patho
- **+ SDD11 Degradation** → next patho
- **+ XTALK** → next patho
- **+ Resonance** → next patho
- **+More Loss** → next patho

First start with pristine loss due to dielectric+skin of real channels, then add other pathologies

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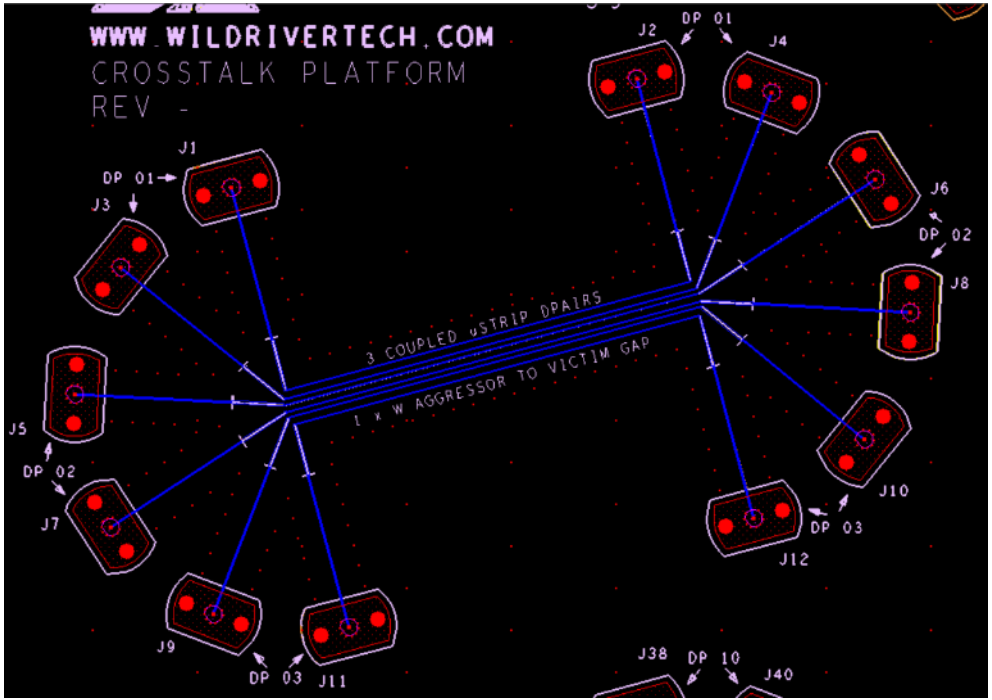
Pathological Design Space – Advancing optimization

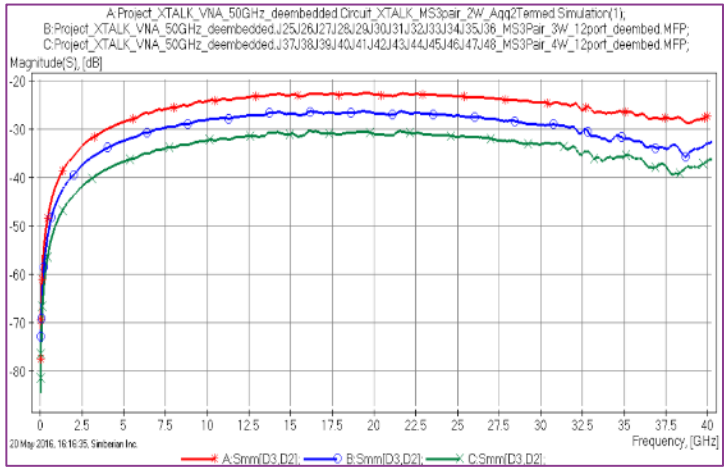


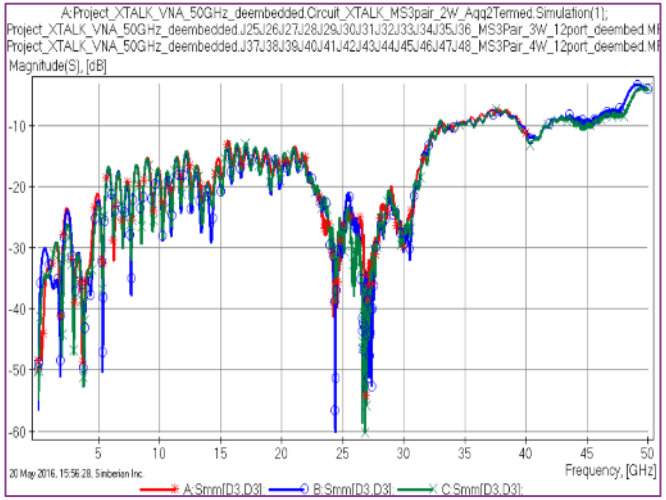
Crosstalk energy at RX also has SDD11 degradation, possible SCD21 (differential to common mode) and possible resonance.

So did the channel have issues due to RX noise due to crosstalk or the other issues?

This structure provides real crosstalk with good S.I.

Pathological Crosstalk Example – Changing FEXT with same SDD11





Sdd[4,1] (FEXT)

Red = 2W Separation
Blue = 3W Separation
Green = 4W Separation

Each crosstalk structure is mapped to the same return loss, SDD11, only RX RMS noise changes

In Summary….

Establishing a Pathological approach uses high-signal integrity structures with isolated issues, and adds those structures in a systematic fashion to establish a channel which serves to improve the methodology of determining margin, and optimization strategies for the modern SERDES

References

- DesignCon2015 Tutorial: Lee Ritchey, Heidi Banes, Chun-Ting “Tim” Wang Lee, Al Neves: **Breaking the 32 Gb/s Barrier: PCB Materials, Simulations, and Measurements**
- DesignCon2014 Presentation: Bob Buxton, Al Neves: **The Role of Improved Measurements and Tools in Assessing Simulation-Measurement Correspondence for 32 Gbps**
- DesignCon2011 Paper: James Bell, Scott McMorrow, Martin Miller, Alfred Neves; **Developing Unified Methods of 3D Electromagnetic Extraction, System Level Channel Modeling, and Robust Jitter Decomposition in Crosstalk Stressed 10 Gbpsec Serial Data Systems**
- **WRT Skew Matched Data Sheets, www.wildrivertech.com**
- **XTALK-28/32 Data Sheet**
- **ISI-28/32 Data Sheet**
- IEEE PG370 TG1, Test Fixture Group Draft 1.0

AGENDA

- Forensic Channel Analysis
- Test Strategies for Pathological Channels
- Gaining Insight with the Pulse Response

Heidi Barnes

SI/PI Applications Engineer
Keysight Technologies

The Well Known Impulse Response

Stimulus

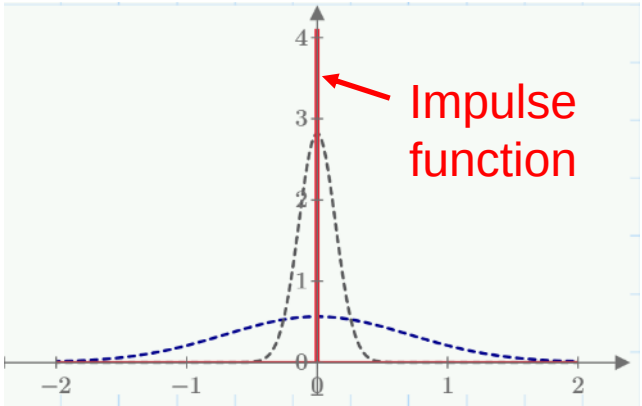
Input: x(t)

Linear Time-Invariant

Response

Output: y(t)

Dirac delta distribution*



*Dirac, Paul (1958), The Principles of Quantum Mechanics (4th ed.), Oxford at the Clarendon Press, ISBN 978-0-19-852011-5.

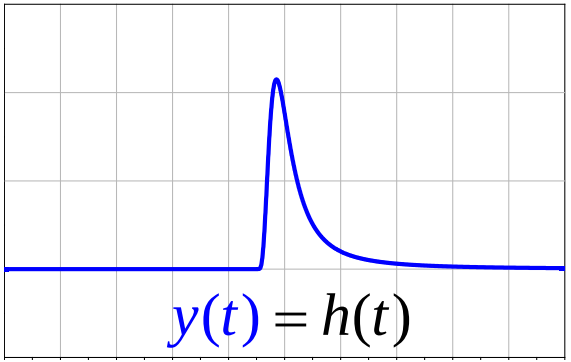
Channel: h(t)

$$y(t) = x(t) * h(t)$$

∗: Convolution operator

In an LTI system, the **impulse response** characterizes the system **completely.**

Impulse Response of the channel

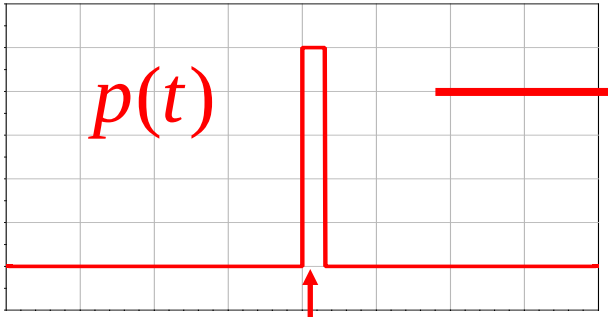


In collaboration with Tim Wang Lee

SI Consultant, Wild River Technologies, University of Colorado

And the Single Bit or Pulse Response

Single **pulse** function

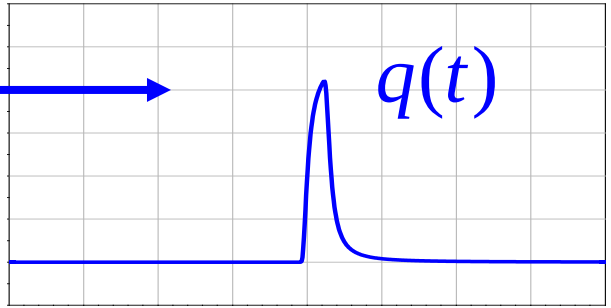


$$width_{pulse} = \frac{1}{\text{data rate}}$$

Linear Time-Invariant

Channel: h(t)

Single **Pulse** Response



$$q(t) = p(t) * h(t)$$

Pulse height: depends (NRZ/PAM4)

When using NRZ, the response is the single **Bit** response.

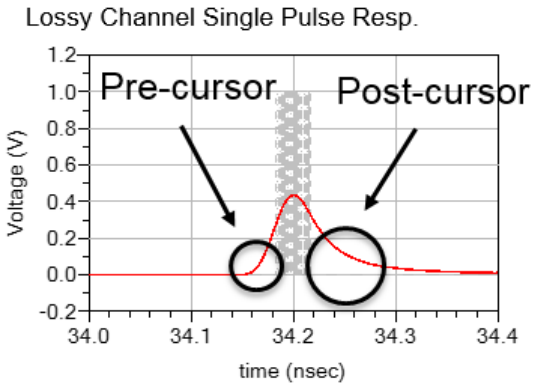
Single pulse response properties:

- Is a deconstructed eye.
- Shows effect of equalization.
- Gives insights to reflection and crosstalk.
- Helps characterize frequency-dependent loss .

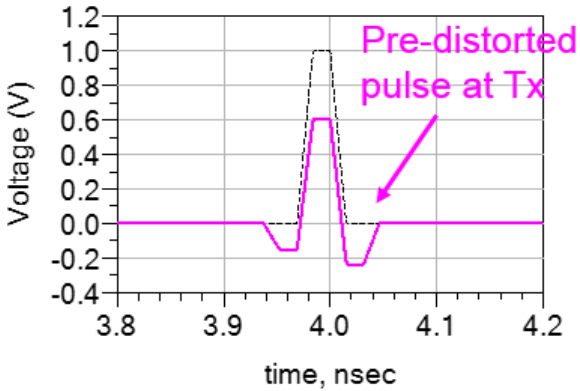
In collaboration with Tim Wang Lee

SI Consultant, Wild River Technologies, University of Colorado

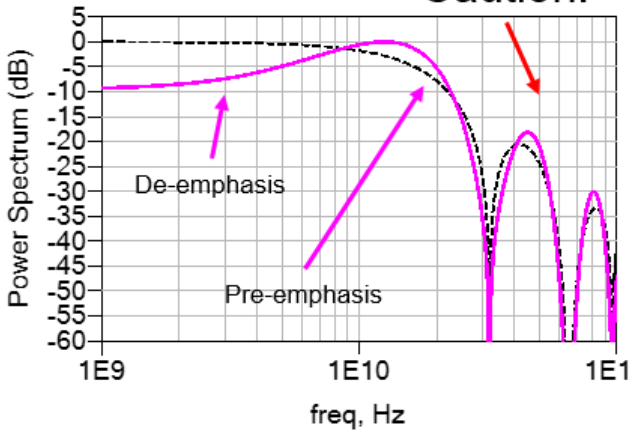
The Pulse Response Shows How the Feed Forward Equalizer Works



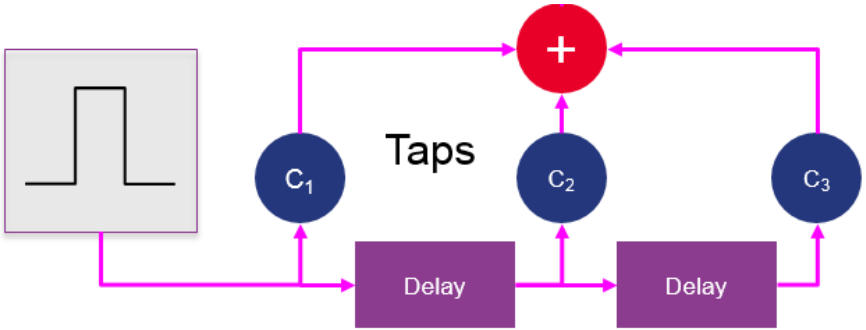
FFE

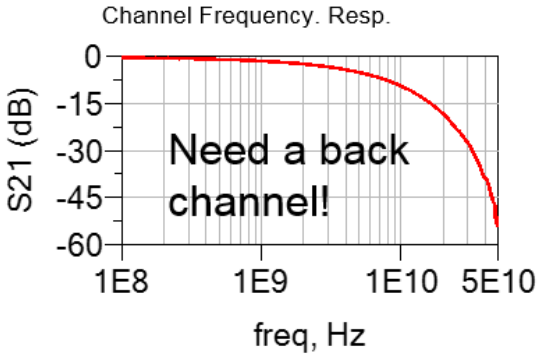


Caution!



Feed Forward Equalizer Algorithm

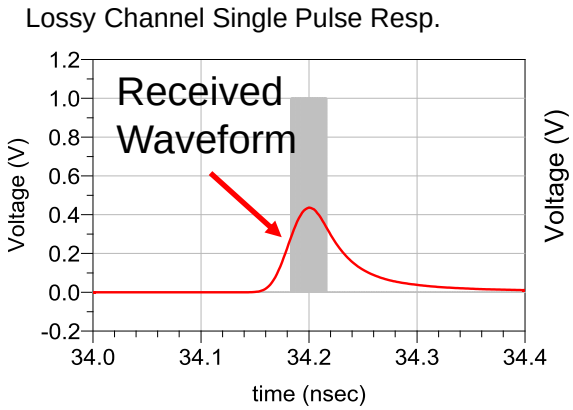


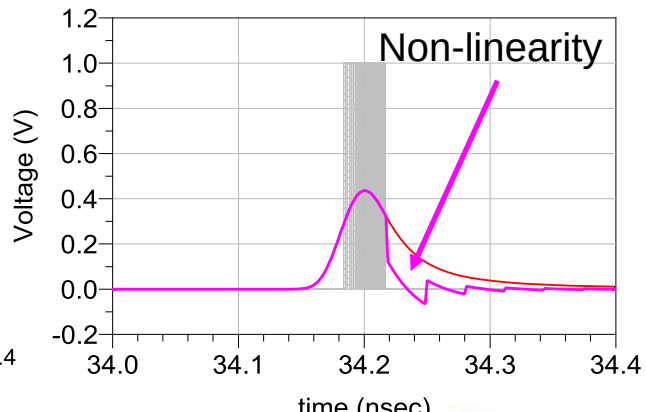


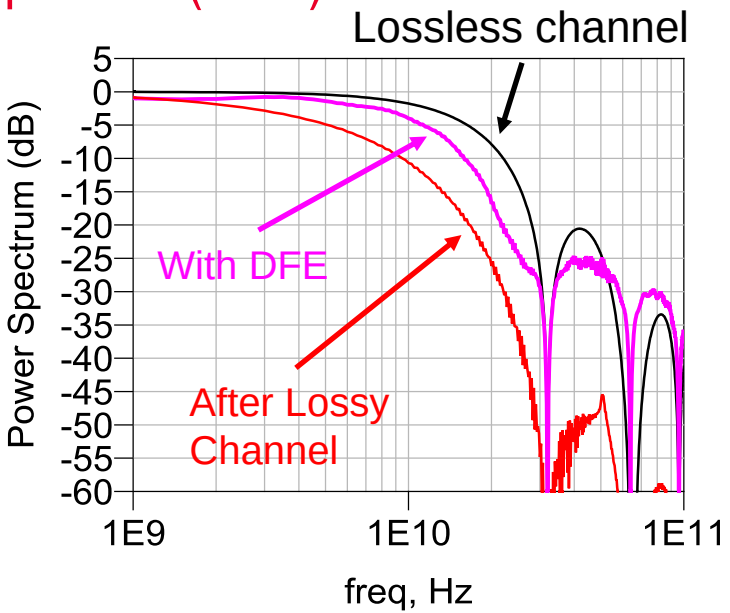
In collaboration with Tim Wang Lee

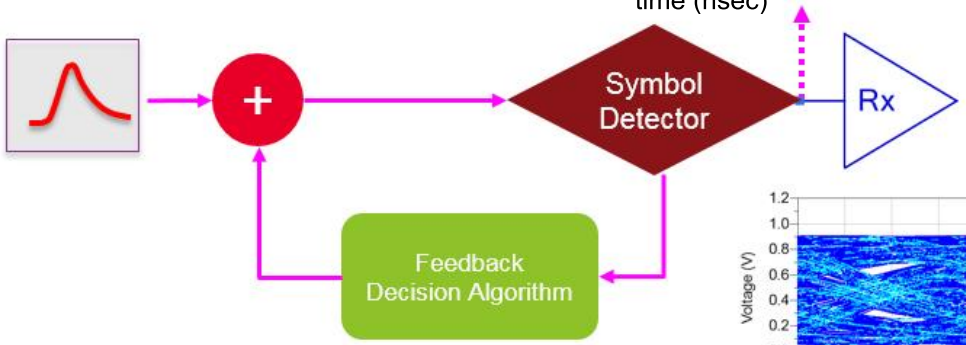
SI Consultant, Wild River Technologies, University of Colorado

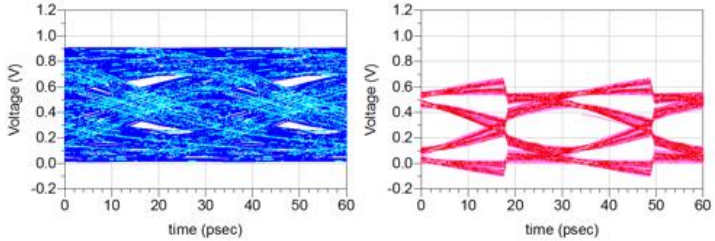
Pulse Response of the Decision Feedback Equalizer (DFE)











In collaboration with Tim Wang Lee

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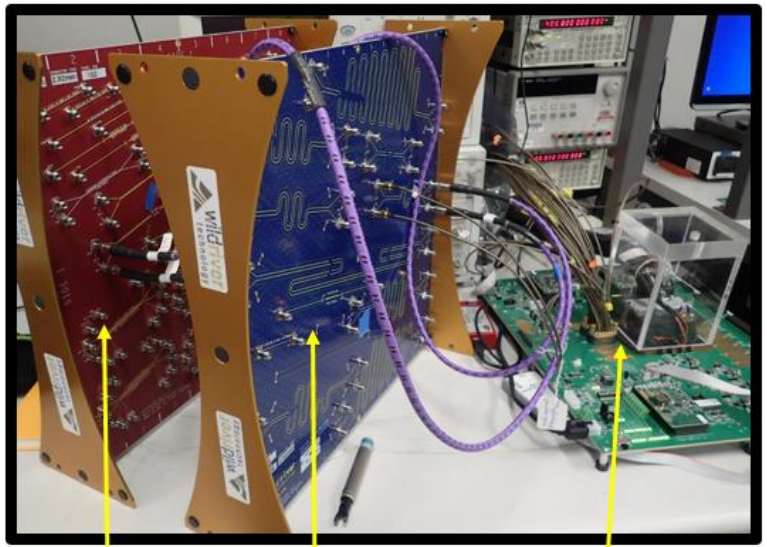
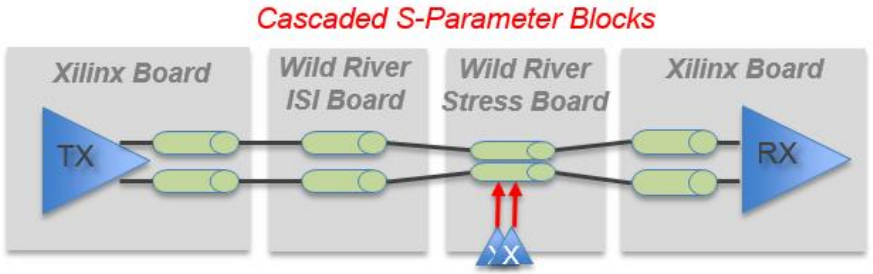
Measuring Band Limited S-Parameters

Simulation requires a cascade of S-Parameters to analyze pathologies.





Do the Rules of Thumb Really Help?

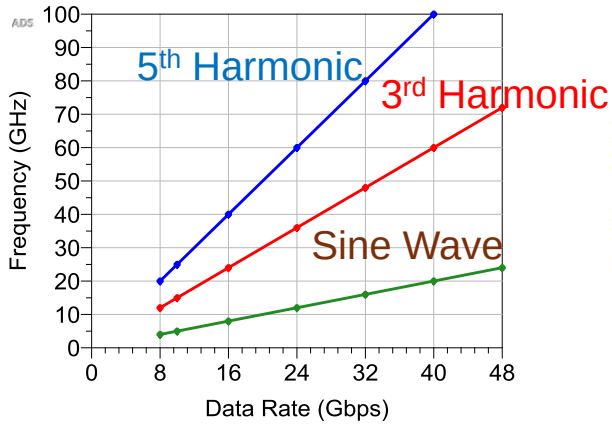
Bandwidth Square Wave
Harmonics

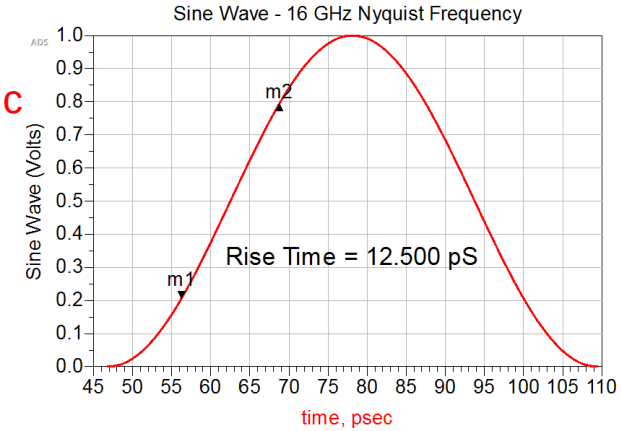
Rise Time Sine Wave

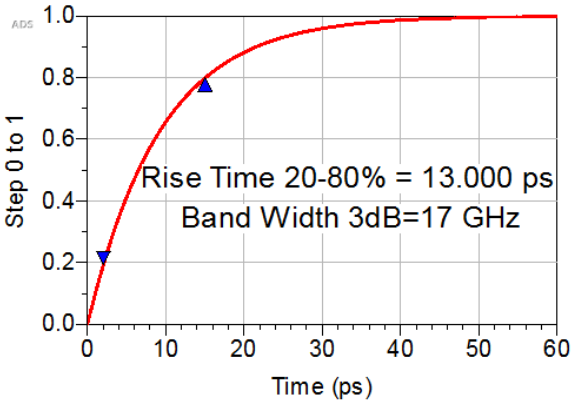
$$Frequency_{Nyquist} = \frac{0.2}{Rise\ Time_{(20\%\ to\ 80\%)}}$$

Bandwidth Step Response
RC Tank Circuit

$$Frequency_{3dB} = \frac{0.22}{Rise\ Time_{(20\%\ to\ 80\%)}}$$



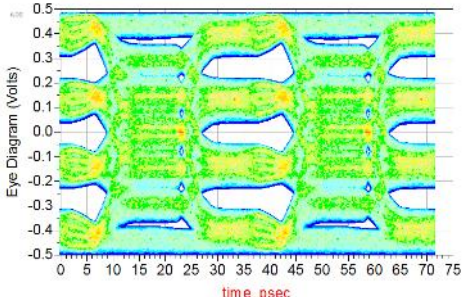


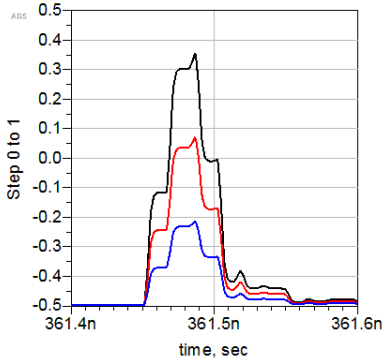


Verify S-Parameter Bandwidth with Simulation

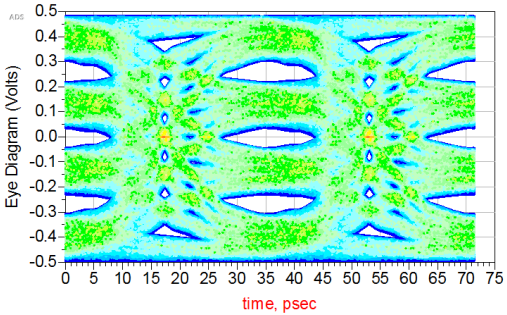
56GBaud PAM-4, 13pS Rise Time Tx, 4.5 in PCB ISI Channel, PRBS15

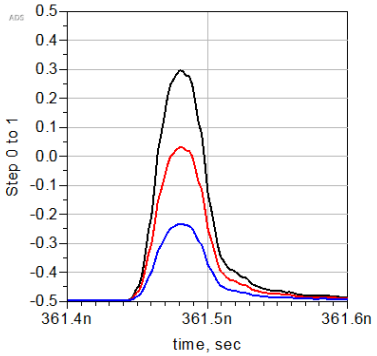
Bandlimited
16 GHz S-Parameters



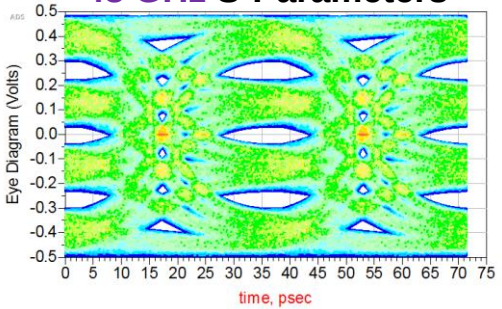


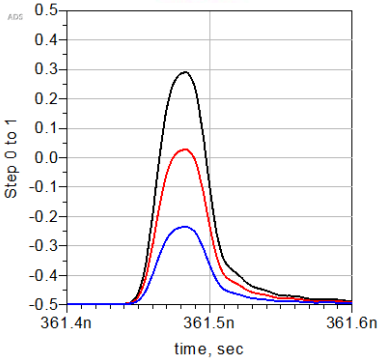
Bandlimited
32 GHz S-Parameters





Bandlimited
48 GHz S-Parameters

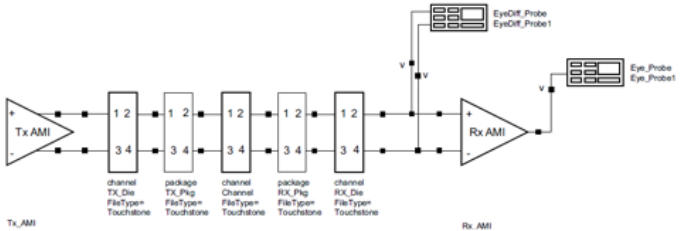




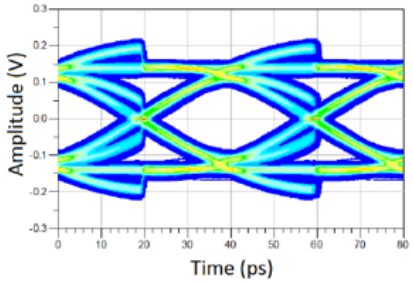
Simulating the SERDES Channel with IBIS AMI Models

Good IBIS AMI Models come with an example for comparison

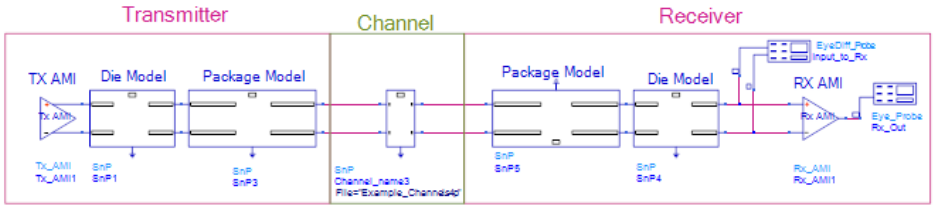
IBIS AMI Kit Example



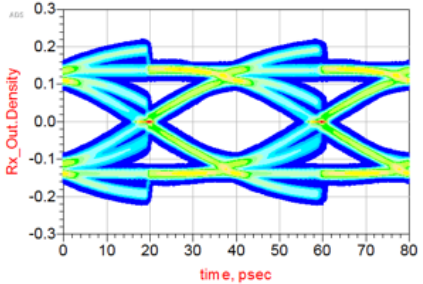
Equalized Eye Diagram



My Simulator Setup



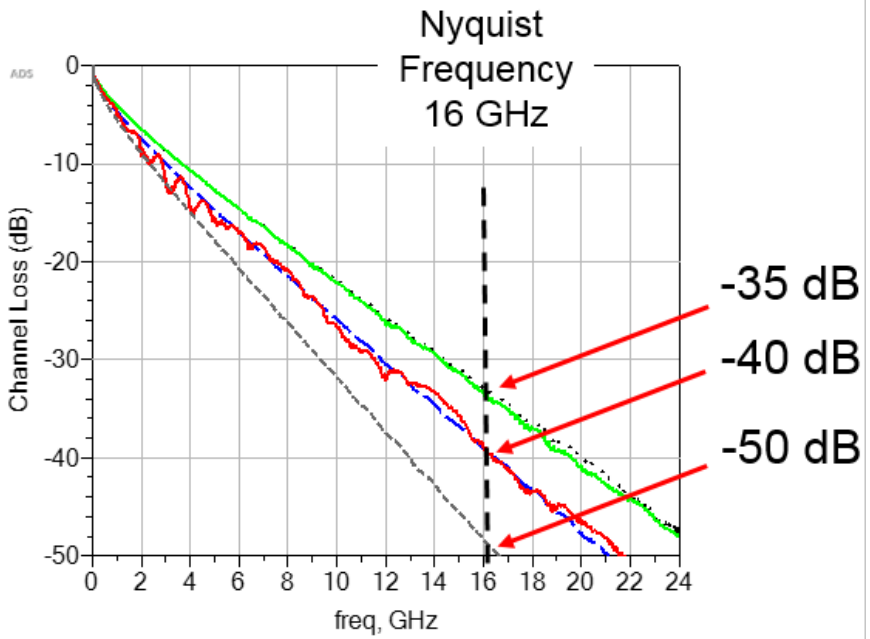
Equalized Eye Diagram



All Loss is Not Created Equal

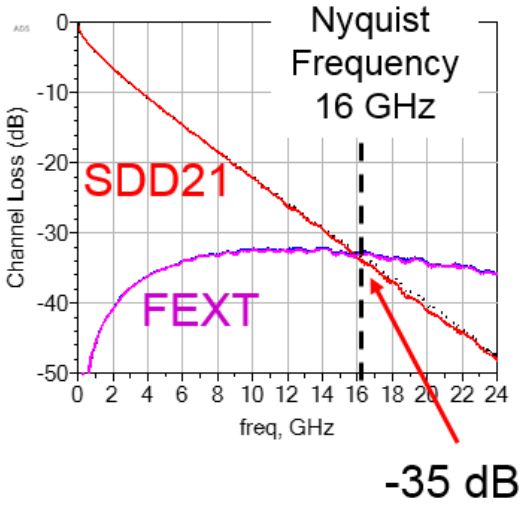
Design of Experiments
3 Types of Signal Degradation

Total Loss	Material Loss	Reflections	XTALK
-35 dB	10in + 4.5in		3W Gap Aggressors
-40 dB	13in +7.25 in	55 and 145 Return Loss	
-50 dB	15.5in + 13in		

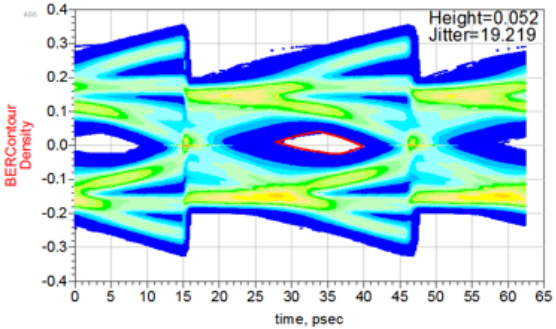


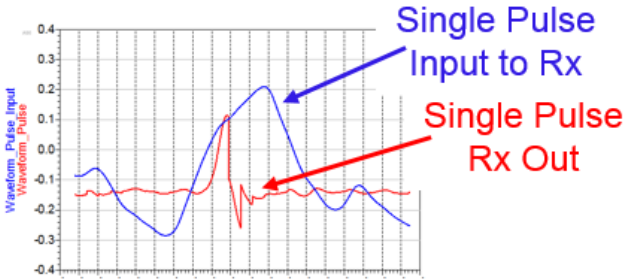
Minimum Tx Equalization Maximizes Signal to Noise

Cross Talk



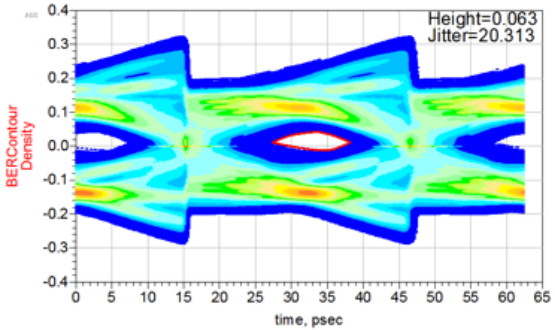
3 dB Tx Precursor with Cross Talk

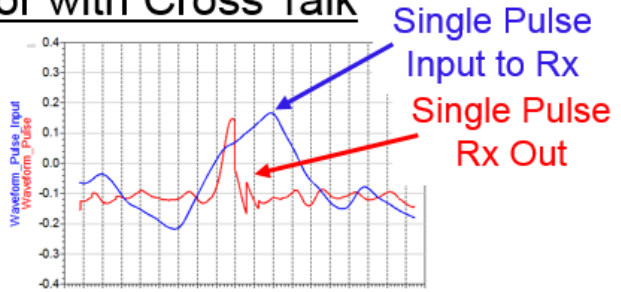




1 UI 31.25 ps per Vertical Grid

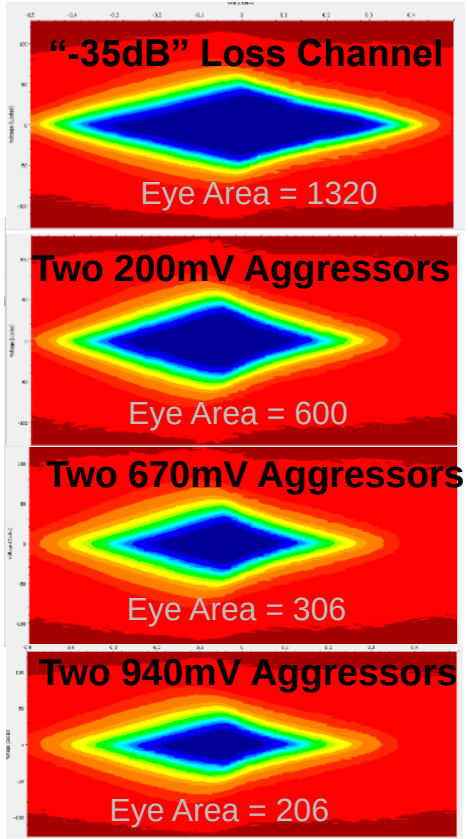
6 dB Tx Precursor with Cross Talk



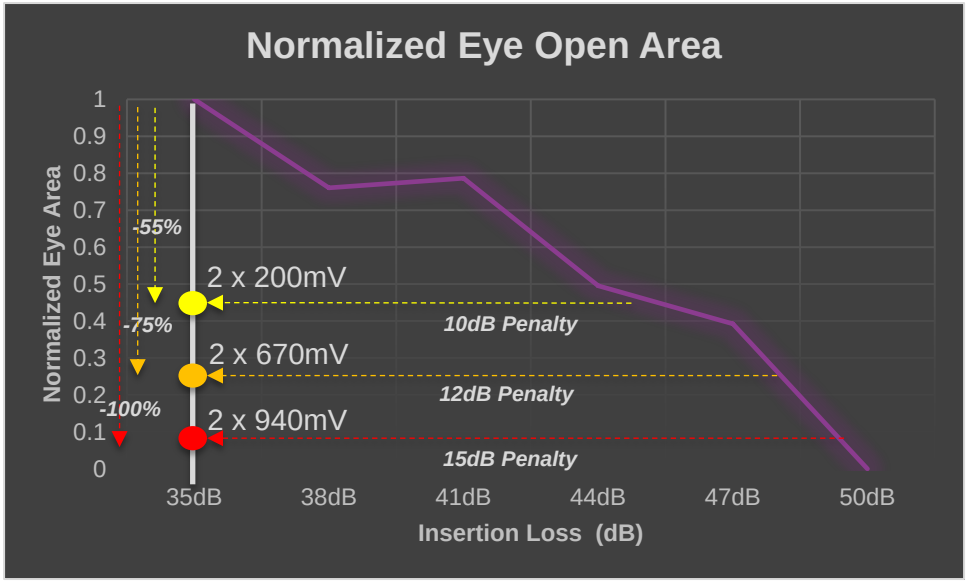


1 UI 31.25 ps per Vertical Grid

Measured Degradation by Cross Talk



32 Gbps, PRBS15, 3dB Tx Precursor, Auto Rx DFE



The Crosstalk also steals the margin for the insertion loss

Measurements by Hong Ahn

SerDes Apps. Engineer, Xilinx

Summary

- The signal integrity of a channel must include analysis of all types of margin eating pathologies such as channel losses, clock noise, and power supply noise.
- A pathological approach breaks down the signal integrity of a SERDES channel to isolate sources of degradation for better optimization of design margins.
- The pulse response can be used to evaluate band-limited S-parameters and equalization techniques. This provides valuable insight for optimizing SerDes channels in the presence of crosstalk.

Thank You! …. And see us all at DesignCon next week!

Tutorial Tuesday Jan. 31st 1:30 to 4:30pm

"32 to 56 Gbps Serial Link Analysis and Optimization Methods for Pathological Channels"

Request a Booth Demo

Keysight Technologies Booth #725

- ADS SIPro and PIPro PCB EM Simulation
- DDR4 Power Aware Transient Simulation
- SERDES Compliance Test Benches
- Xilinx PAM4 Measurement and Simulation

Wild River Technology Booth #850

- Technology Development Platform 50GHz
- Check out our latest Hermetic Cables to 50GHz
- 70GHz Test Fixture Design
- CCIX Xilinx Demo

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